Persistent Memory Objects on the Cheap

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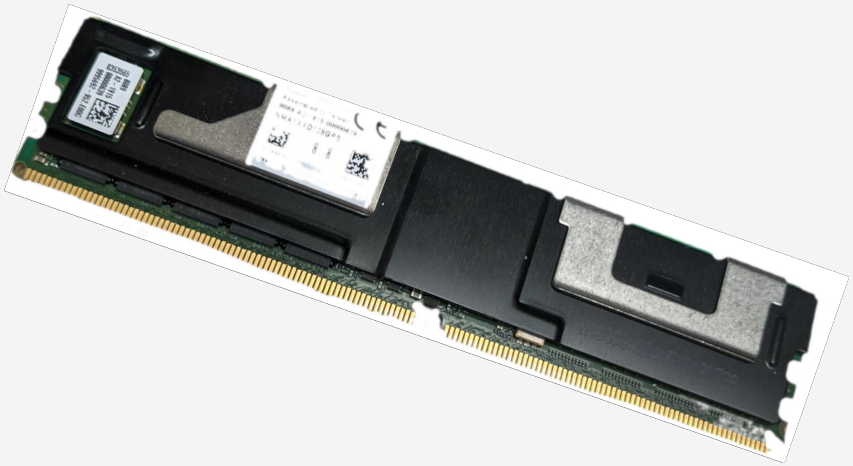
Overview

Persistent Memory (PM)

Example: Intel Optane, CXL Memory-Semantic SSDs



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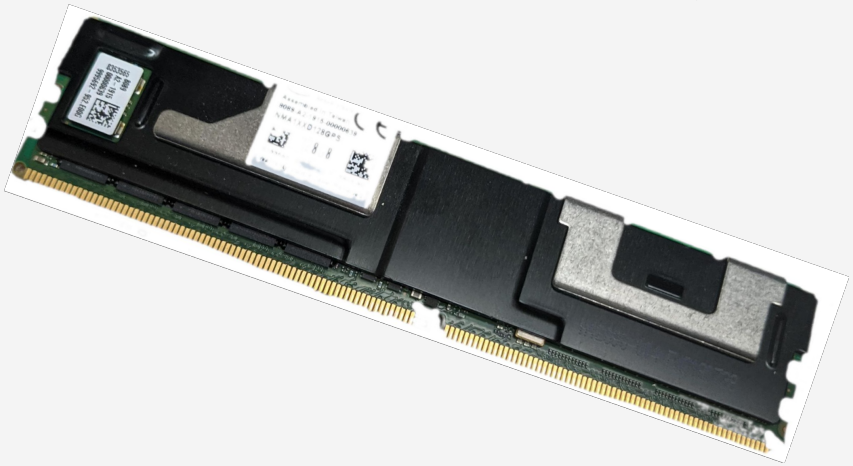

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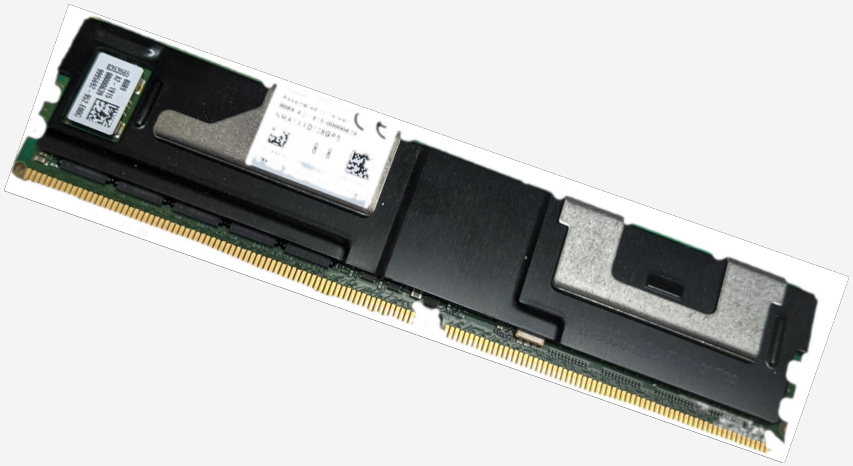

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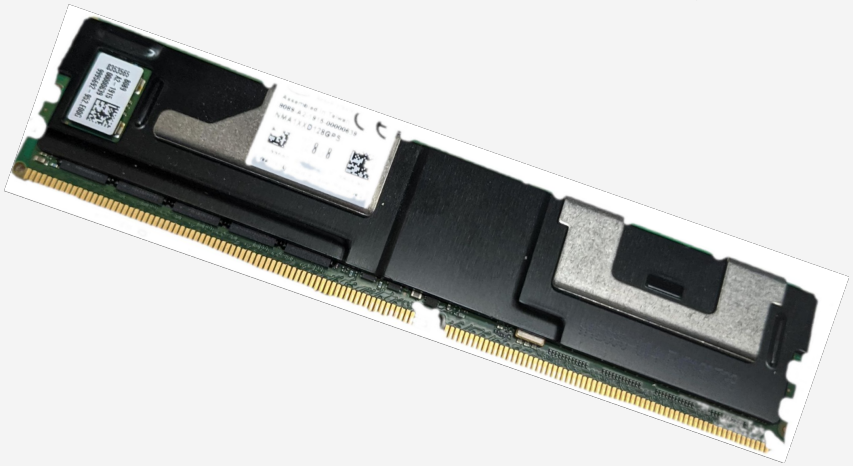

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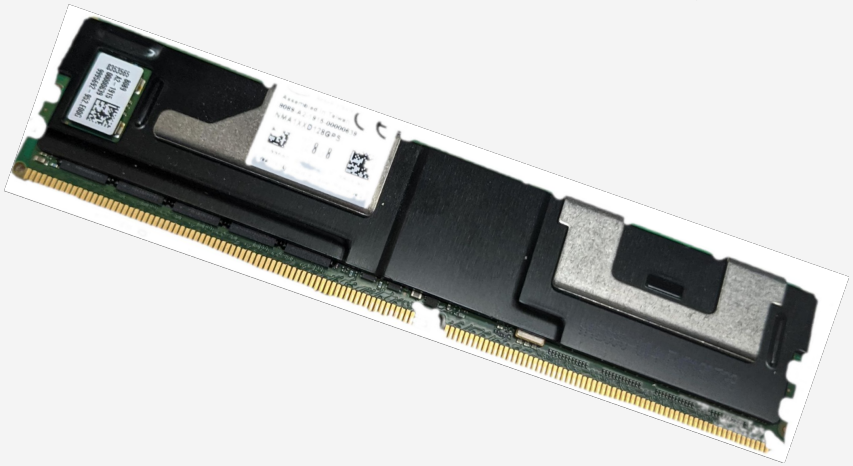

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Note: Devices with PM usually have DRAM as well

Persistent Memory Objects (PMOs)

Primitives: pcreate()

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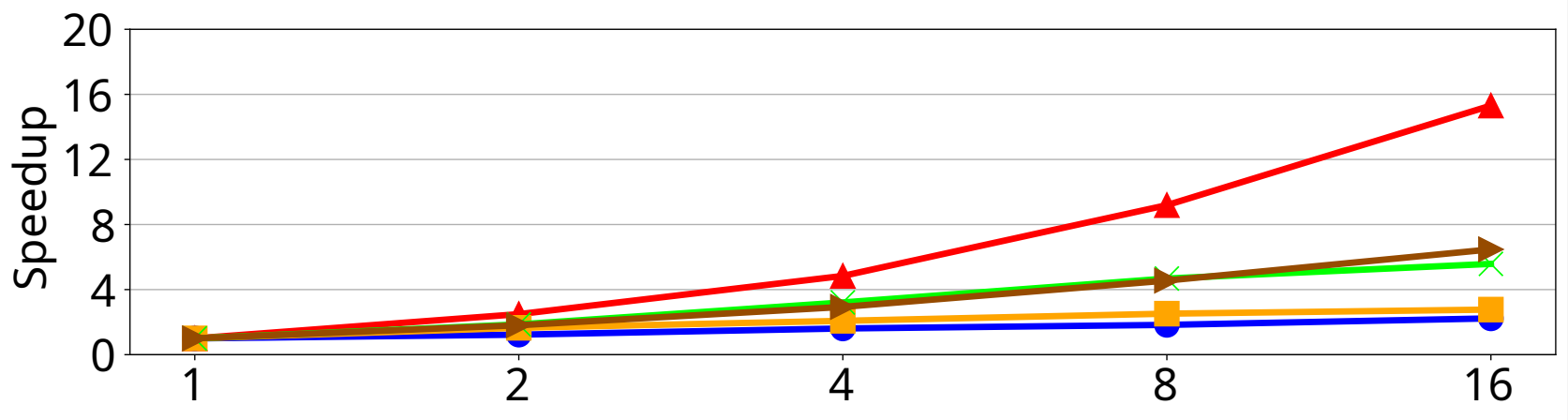

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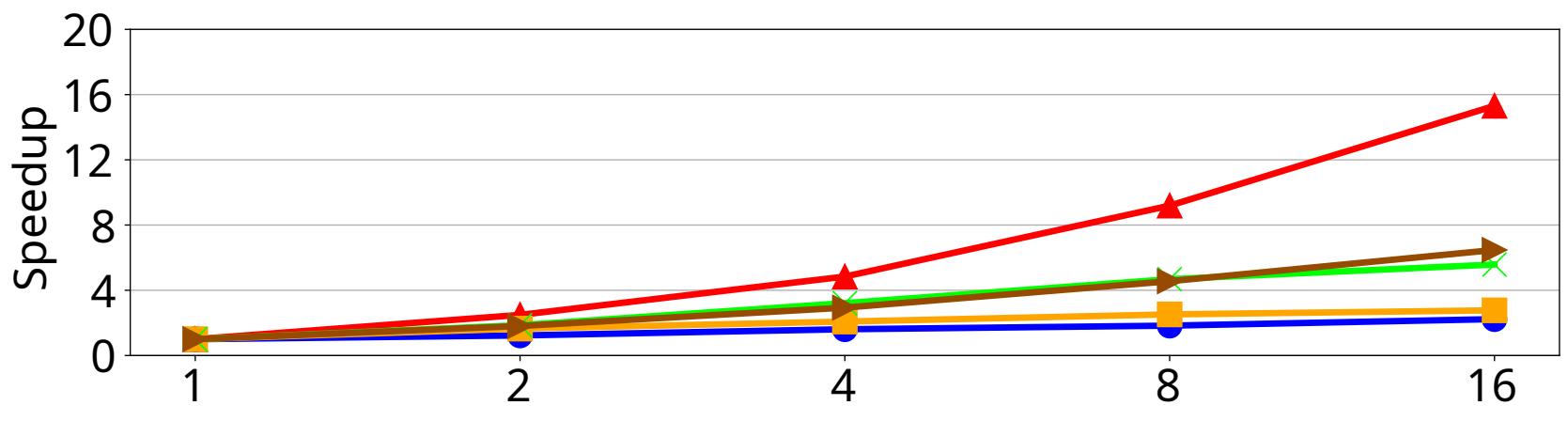

Reasons

- PMOs are hosted entirely in PM

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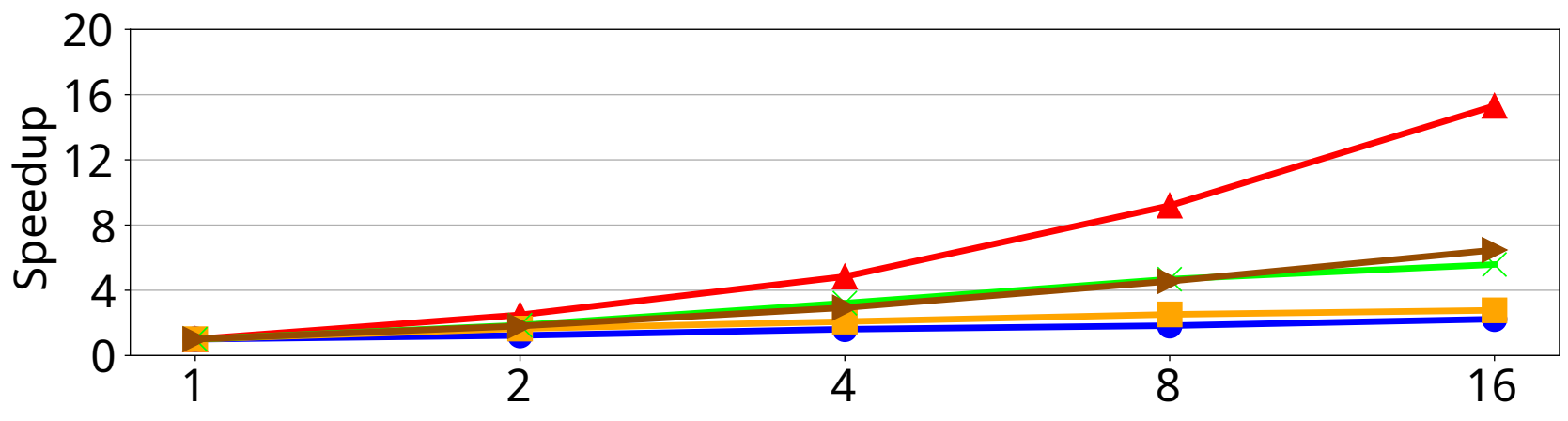

Reasons

- PMOs are hosted entirely in PM
- Encryption and integrity verification on the critical path

CXL Devices

CXL: SOTA for PM

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Compute Express Link

- Utilizes PCIe interface
- Direct access from CPU to memory
- Heterogeneous memory pools
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Goal: High-Performance PMOs

CXL at-rest encryption

There is a way to do this...

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CXL 3.1 Specification

- Trusted Execution Environments (TEE) Security Protocol (TSP)

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Overview

Threat Model

Goal: Protect at-rest data from disclosure/corruption

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Out of Scope

- Side-channel attacks
- Data-remanence attacks (DRAM)

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DRAM as cache = Reconfigurable Memory

Reconfigurable Memory Hierarchy

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- Primary and shadow in plaintext

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- Primary and shadow page encrypted
- Primary and shadow in plaintext
- **Shadow in plaintext, primary in ciphertext**

Reconfigurable Memory Hierarchy (Part 2)

Optane PM uses local DRAM

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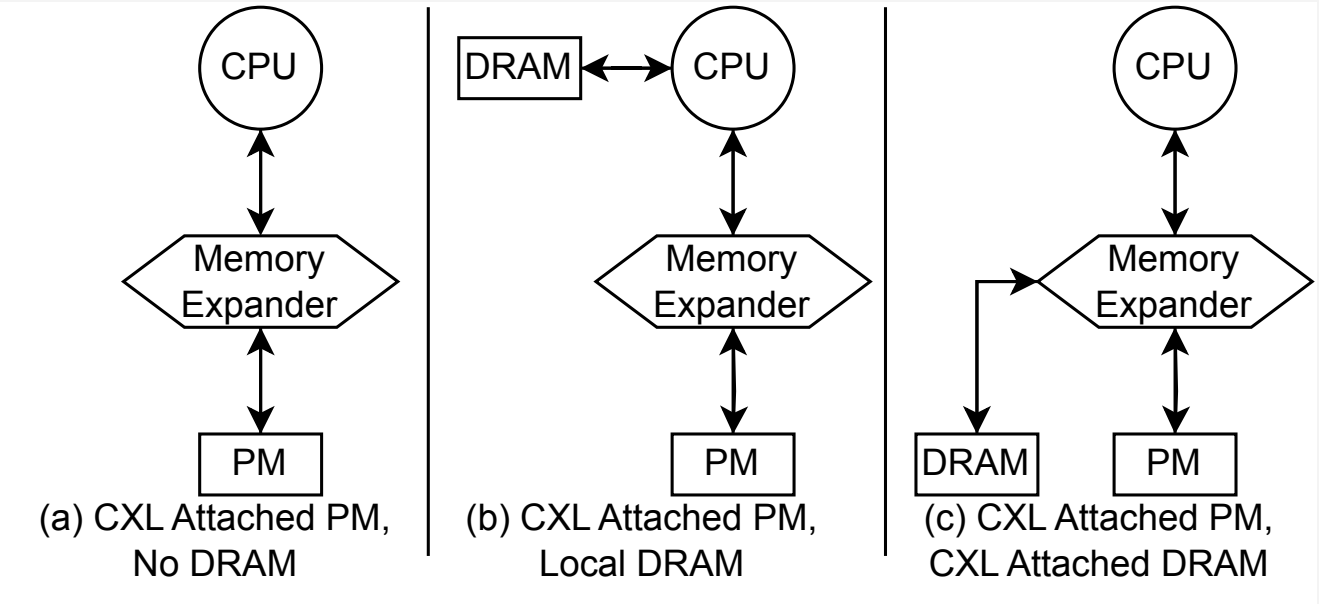

CXL can place system on either side of memory expander

Reduce page fault latency

Prior work: Demand Faulting

Why not **predict** when pages are needed?

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Why not **predict** when pages are needed?

Example Solution: Stream Buffer

- On fault, predict next X sequential pages (**depth**)
- Works well for access patterns amenable to prediction

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Evaluation

Evaluated Benchmarks

- Microbenchmarks
  - 2d Convolution (2dConv)
  - Gaussian Elimination (Gauss)
  - LU Decomposition (LU)
  - Tiled Matrix Matrix Multiplication (TMM)
- Filebench (Fileserver, VarMail, WebProxy, WebServer)
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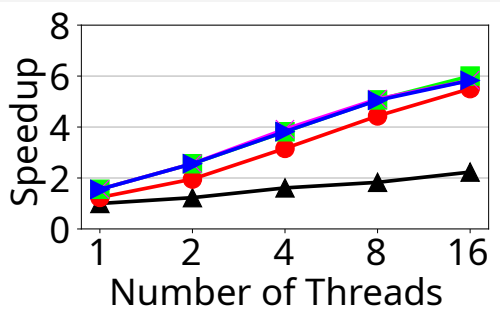
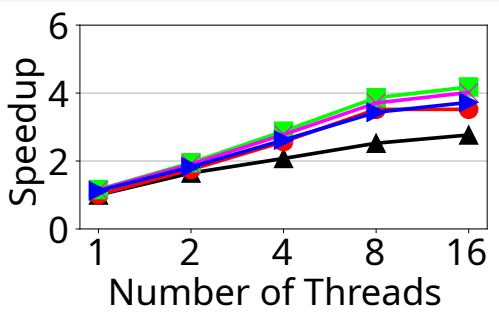
Component	Specifications
MB	Supermicro X11DPi-NT
CPU	2×Intel Xeon Gold 6230 (20 cores)
DRAM	4 × 32GiB DDR4 @ 2666MHz
PM	4 × 128GiB Intel Optane DIMM
OS	AlmaLinux 9.0; Linux 5.15.157

LPMO Performance

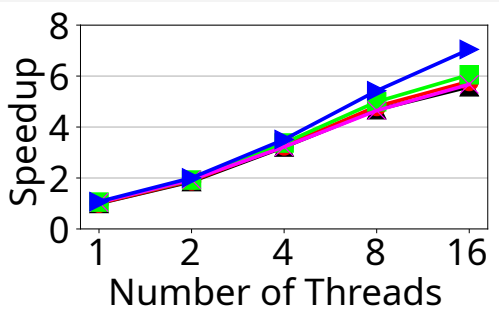
△ O, ○ D, □ D2, × D4, ▷ D8



(a) Gauss



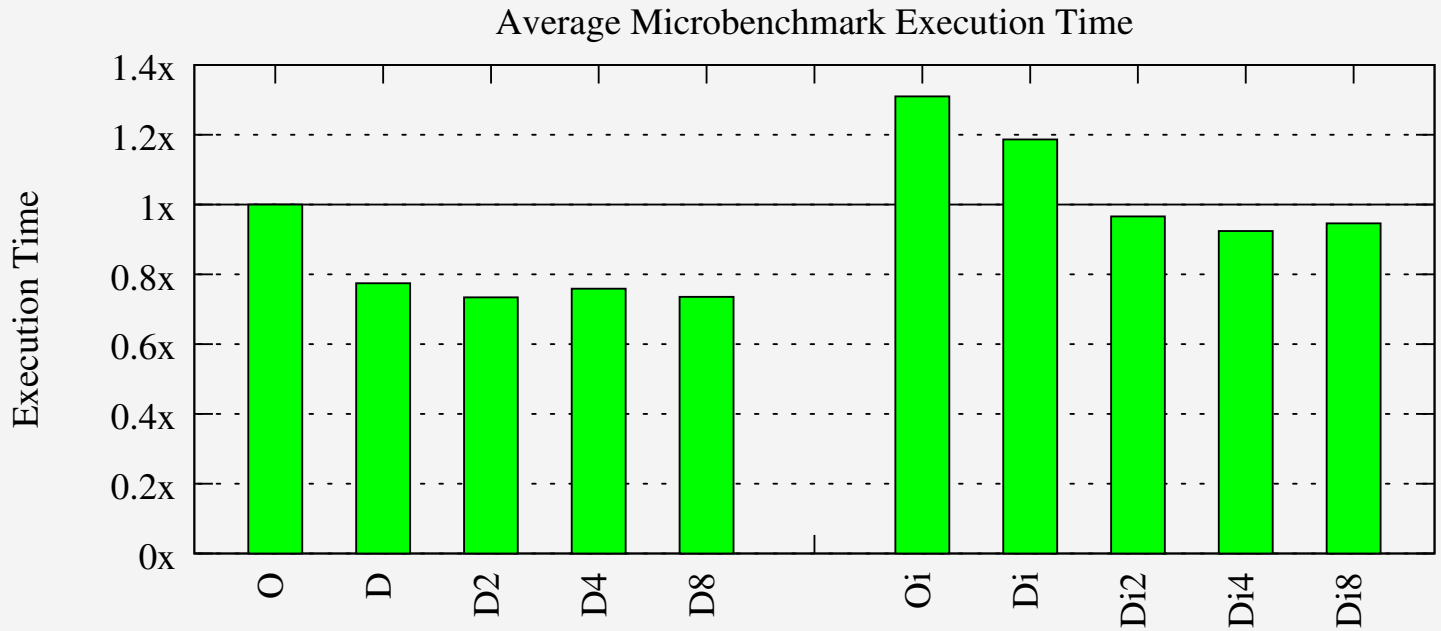
(b) LU



(c) TMM

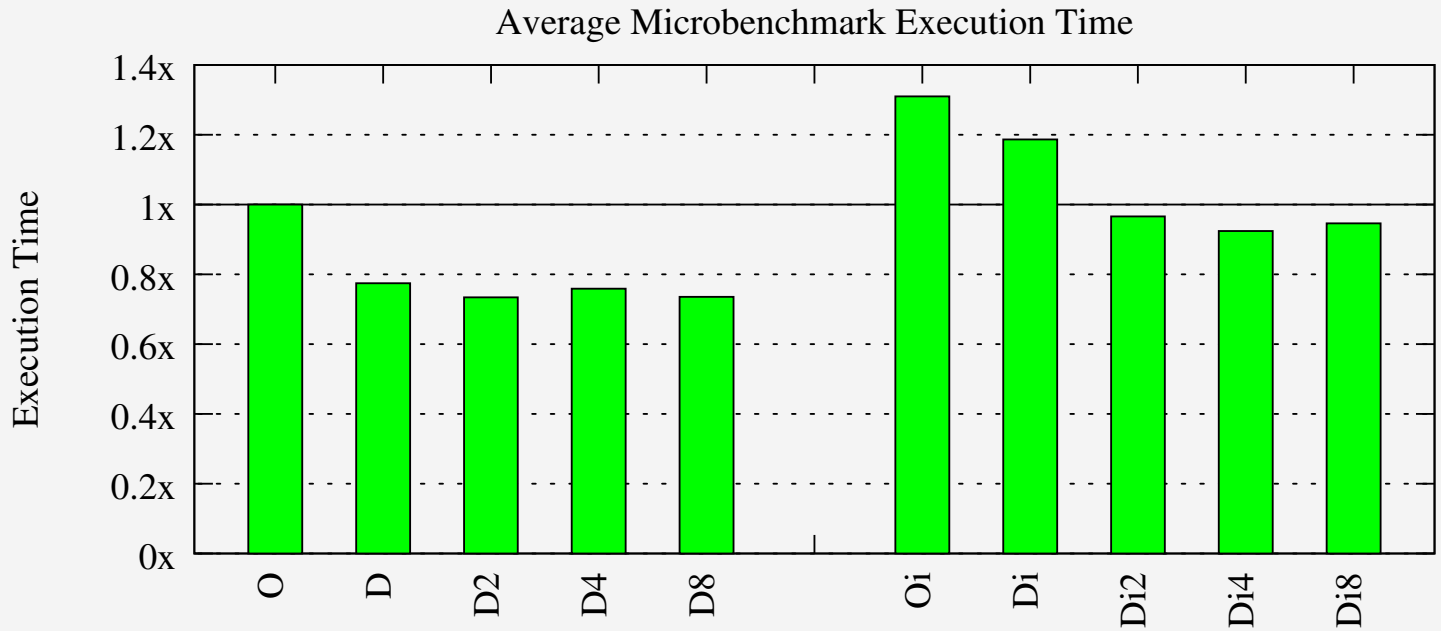
All benchmarks have better thread scaling!

LPMO Performance



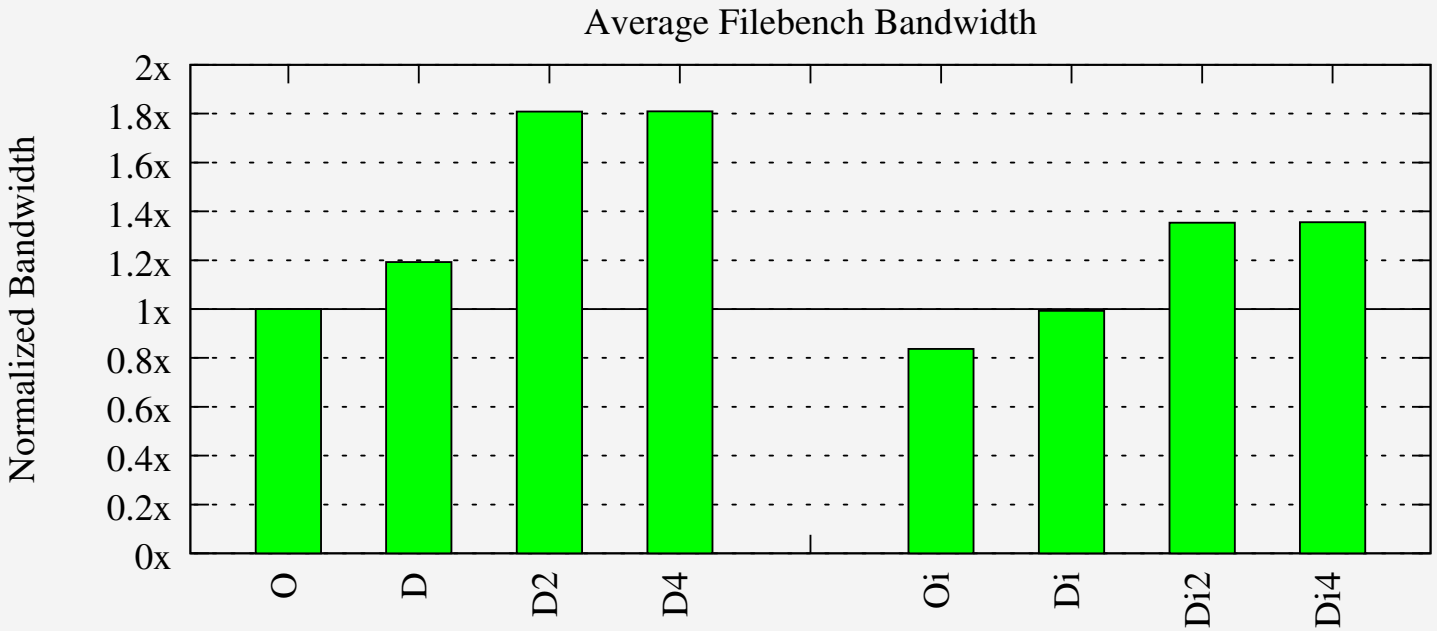
- DRAM reduces execution time by $\approx 21\%$

LPMO Performance



- DRAM reduces execution time by $\approx 21\%$
- IV + Prediction faster than original GPMO design w/o IV

LPMO Performance - Filebench



- Only 1.19× faster with DRAM

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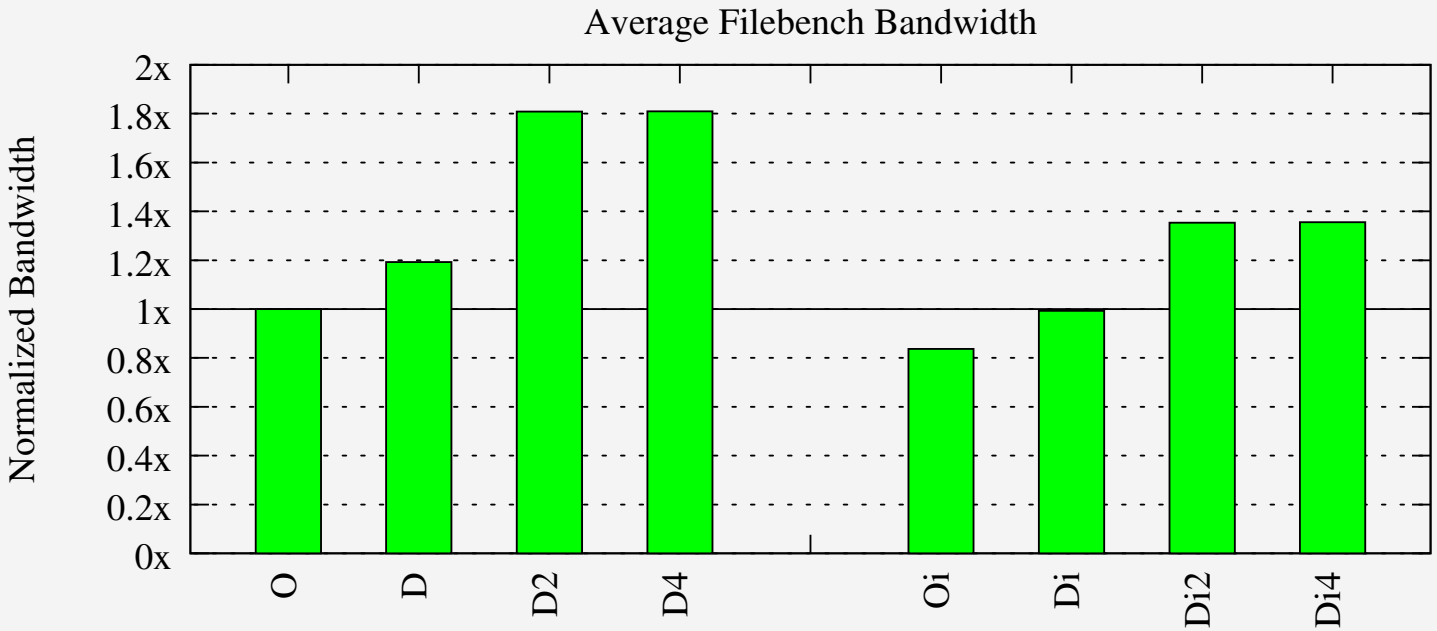

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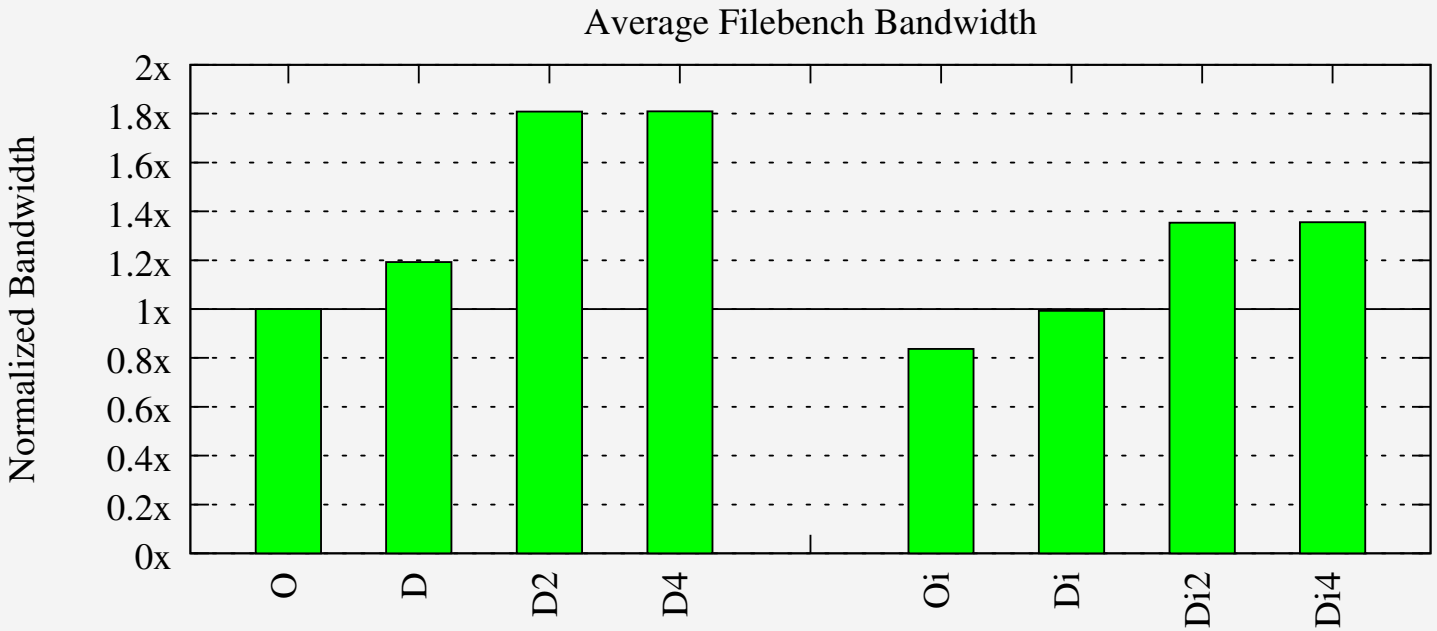

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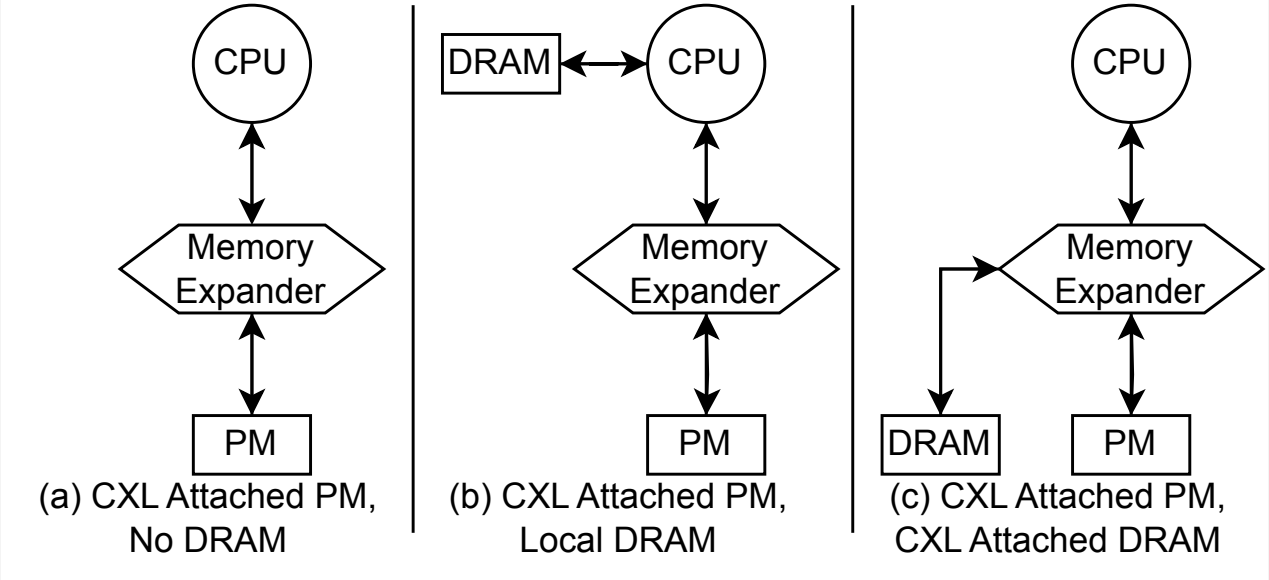
- 1.81× **faster with page prediction**
- 1.37× faster with page prediction & **IV**

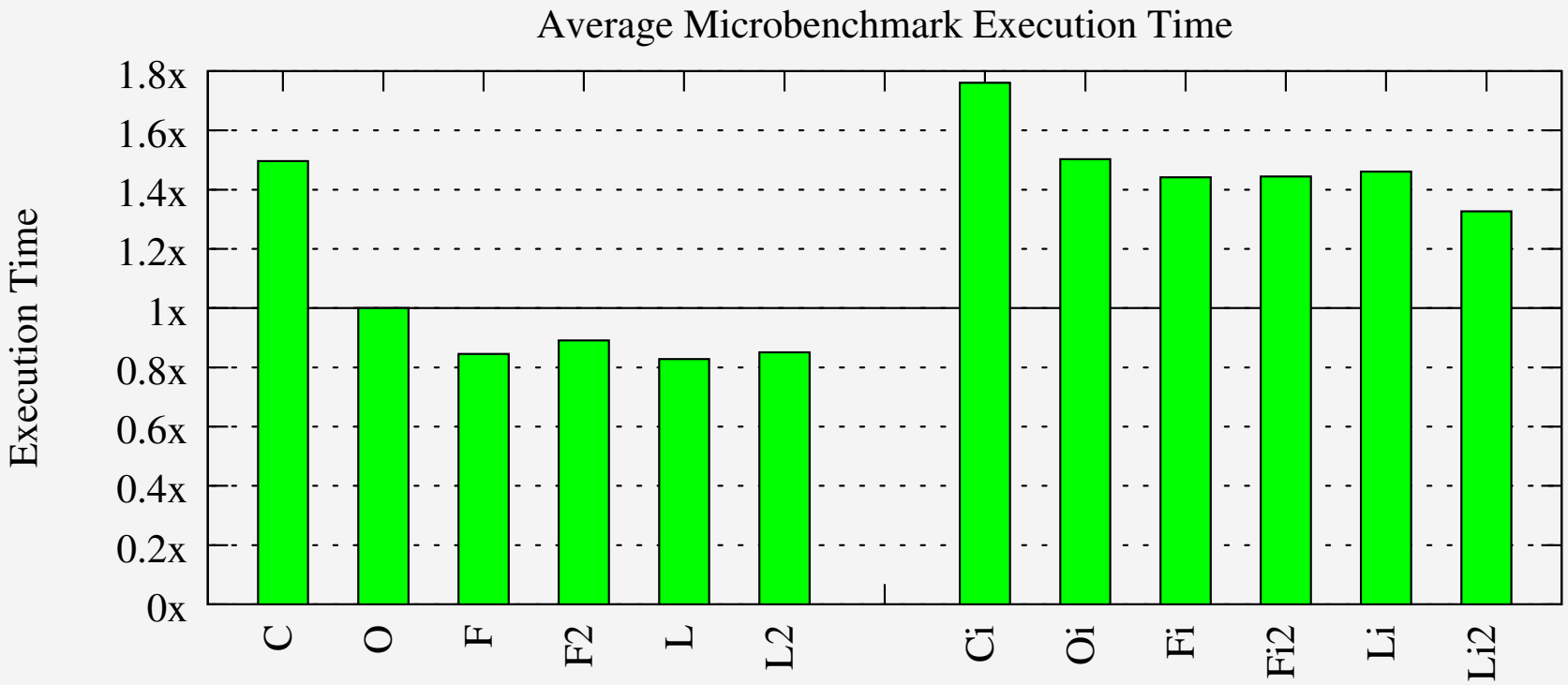
CXL Performance

Perform same tests, but emulate CXL latency



- Use opposite-node Optane
- Near configuration: cache allocated from local node
- Far configuration: cache allocated from opposite node

CXL Performance



(Lower is better)

- With CXL alone: 50% slower than original
- With DRAM: 20% faster (despite CXL latency)

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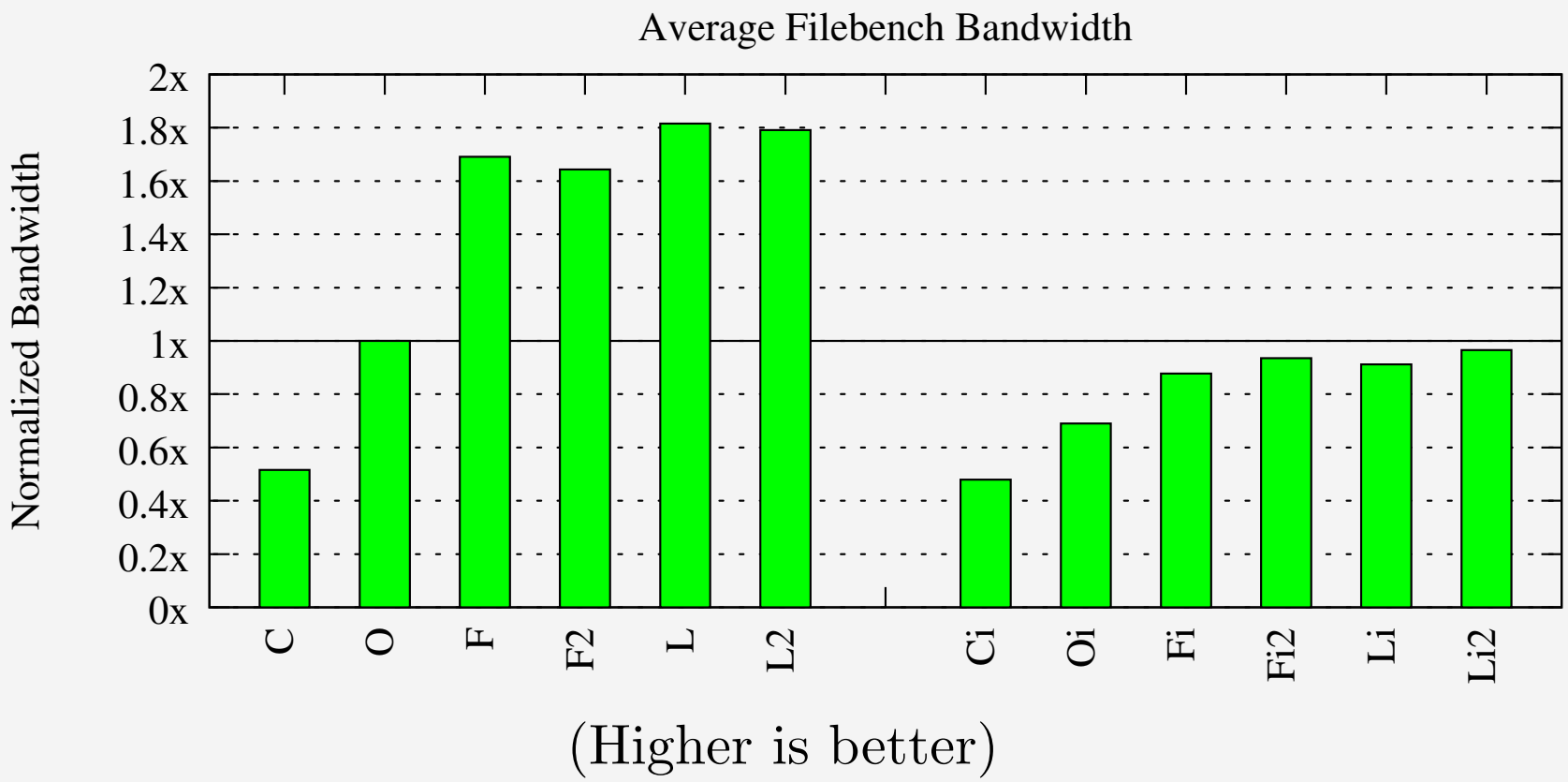

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- Introduced Reconfigurable Memory Hierarchy
- CXL latency can be masked by LPMO optimizations

Q & A

Thank You!

Any questions?